FPGA based control circuit for DC potential biasing of electrodes in two stages.

Abstract

Abstract:To destructively analyse the parallel energy of the non-neutral electron plasma of SMARTEX-C experimental setup, an FPGA based two-stage dump circuit needs to be designed. Energetic electrons will escape the plasma when end-grid potential (-V0) will be raised by ?V (stage-I), electrons thus escaped will be measured on the charge collector and remaining plasma will be dumped and measured by raising the potential of the end-grid to (V1) positive potential (stage-II). These two-stage dump will be repeated by incrementally increasing ?V to construct the energy distribution function. Electronically, pulsing of high voltage ranging from -V0 (few 100's of V) to +V1 (few 10's of V) needs to be done by power amplifiers, timing of these pulses will be programmed with FPGA and controlled via LabView. Charge collection will be carried out by capacitive charging circuit consisting of highly filtered positive bias and amplifier to measure the tiny charge. Data will be transferred to Data Acquisition System and analysis of the data to construct distribution function will be carried out. LabVIEW based graphical user interface needs to be developed which comprises of voltage range, timing sequence, step increment and other necessary control parameters. Interface of hardware with PC will be carried out through Ethernet based protocol.

Academic Project Requirements:

1) Required No. of student(s) for academic project: 1

2) Name of course with branch/discipline: B.E./B.Tech. Electronics and Instrumentation Engineering

3) Academic Project duration:

(a) Total academic project duration: 9 Weeks
(b) Student's presence at IPR for academic project work: 5 Full working Days per week

Email to: minsha@ipr.res.in[Guide's e-mail address] and
project_ece@ipr.res.in [Academic Project Coordinator's e-mail address]

Phone Number: 079 -07923962124 [Guide's phone number]